LPRDS-CMS 2011
Lafayette Photovoltaic Research and Development System: Cell Management System

ECE 492 – 2011

Acceptance Test Plan

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Last Revision 04/20/11 by Greg Earle

Requirement	Applicable/Modification	Confirmation Method	Achieved
R002-2	We are developing a new design for per-cell battery management.	Demonstration of convergence of a 4-cell pack as per **Test T001** which will run ten (10) charge/ discharge cycles	✓
R002-3	We are only charging one pack, not the entire system.	Using resistive bypass, over ten (10) charge/discharge cycles, measurement of voltages and SOC via Simulink will demonstrate per-cell balancing as per **Test T001**	✓
R002-4	Applicable	Using Simulink, a discharge curve will be created to demonstrate that over-discharge does not occur as per **Test T001**	✓
R002-5	Applicable	Visual demonstration of OBPP will confirm operational "stand-alone" state via LED indicators during **Test T001 & Test T002**	✓
R002-6	I2C is used to monitor in detail voltage, current, and SOC of battery pack, including every individual cell.	I2C interface will be utilized during **Test T002** to monitor the voltage, current, temperature and SOC of each individual cell in the pack via a PC terminal application	UNCALIBRATED BUT WORKS
R002-8	Applicable	**Final Report** will include photographic evidence of usage of existing LiFePO4 cells	✓
GPR001-1	Applicable	~~See QA Audit Report for list of~~ documentation ~~and locations~~	✓ is fully indexed on the website
GPR001-2	Applicable	~~The team has comprised a~~ **Standards Document**, which is ~~located on the~~ project website. Another member of the team will edit each individual's work to ensure adherence to group standards, compliant with those of Lafayette College writing courses.	✓
GPR001-3	Applicable	Inspection	✓
GPR001-4	Applicable	Inspection of **QA Audit Report** and low-level test reports	✓
GPR001-5	Applicable	All schematics, mechanical drawings, circuit net-lists, BOMs, artwork, assembly drawings and other files necessary for manufacturing are located on the	✓

		Project Website under the tab "**Resources**" -> "**OBPP Design Documents**"	
GPR001-6	Applicable	All datasheets of components used in the system design are located on the **project website** under the tab "**Resources**" -> "**Datasheets**"	✓
GPR001-7	Applicable	The final report will include a section entitled **Firmware Development** which will include documentation of the design decisions, implementation and issues with the current firmware	✓
GPR001-8	Applicable	See User's Manual located on **Project Website** under the tab "**Project Documents**"	✓
GPR001-9	Applicable	See Maintenance Manual on **Project Website** under the tab "**Project Documents**"	✓
GPR001-10	Applicable	Inspection of **Project Website**. All files to be delivered are in standard and portable document formats.	✓
GPR002-1	Applicable	**SWR001-1**: **Environmental Memo** (in the **Final Report**) will analyze that the system meets the operational and storage temperatures. In addition, RoHS compliance will be analyzed.	✓
GPR003-1	Applicable	**SWR001-2**: **EMI/EMC Memo** (in the **Final Report**) will analyze the unintentional electromagnetic radiation concerns of the system	✗ UNACCEPTABLE
GPR004-1	Applicable	**Environmental Memo** will analyze if the system has any hazardous materials and if they comply with LC Chemical Hygiene Plan	✓
GPR004-2	Applicable	**Environmental Memo** will make sure all materials used in electronic circuit fabrication are RoHS compliant	✓
GPR004-3	Applicable	**Environmental Memo** will consider disposal of design or prototypes	✓
GPR005-1	Applicable	Inspection	✓

GPR005-2	Applicable	Firmware will be peer reviewed to ensure that it complies with all principles and practices established in LC's course CS205 Archived revision histories (zip files) and final version of PIC firmware will be located on the project website under **"Resources" -> "PIC Firmware"** tab. Testing software (Simulink files) for ATP/ATR will be located on the project website under **"Resources" -> "Test Software"** tab. A Software Readme file will be located on the project website under the **"Resources"** tab.	✓
GPR005-4	Applicable	A jumper connection on the board (Ref Des) will reset the board when the contacts are bridged.	✓
GPR005-5	Applicable	See **Voltage Analysis Memo** in **Final Report**	✓
GPR005-6	Applicable	See **Power Dissipation Memo** in **Final Report**	✓
GPR005-8	Surface temperature rise no greater than 70 degrees C above ambient	**Test T001** demonstrates that the components used do not have a surface temp > 70°C above ambient (30°C)	✓
GPR005-9	Applicable	See **Power Dissipation Memo** in **Final Report**	✓
GPR005-10	Applicable	See **Voltage Analysis Memo** in **Final Report**	✓
GPR005-11	Applicable	See **Maintenance Manual** on **Project Website** under "**Project Documents**"	✓
GPR006-1	Applicable	See **Reliability Memo** in **Final Report**	✓
GPR006-2	Applicable	See **Reliability Memo** in **Final Report**	✓
GPR006-3	Applicable	See **Reliability Memo** in **Final Report**	✓
GPR006-4	Applicable	**Tests T001** will be conducted within a 24-hour period of continuous system operation.	✓

GPR006-5	Applicable	See **Reliability Memo** in **Final Report**	✓
GPR007-1	Applicable	See **Maintainability Memo** in **Final Report**	✓
GPR007-2	Applicable	See **Maintainability Memo** in **Final Report**	✓
GPR007-3	Applicable	See **ATP** for spare parts list, **User's Manual** for troubleshooting procedures, and **Maintenance Manual** for more elaborate diagnosis and troubleshooting resources. All docs are located on **Project Website** under "**Project Documents**"	✓
GPR007-4	Applicable	**Test T003** will check the usefulness of the User and Maintenance Manuals	✓
GPR008-1	Applicable	See **Manufacturability Memo** in **Final Report**	✓ WEAK
GPR008-2	Applicable	See **Manufacturability Memo** in **Final Report**	✓
GPR011-1	Applicable	Final Project demonstration will take place on 5/6/11 for ECE Faculty	✓
GPR012	Applicable	Inspection	✓

Acceptance Testing Approved:

X _____ 5/6/11

X _____ 6 May 2011

Acceptance Test Report

Deliverables	Due Date	Completed	Initials	Date
D001: CDR Materials	3/2/2011	✓		5/3/11
D002: User's Manual	5/6/2011	✓		5/6/11
D003: Final Report and Maintenance Manual	5/6/2011	✓		5/6/11
D004: Acceptance Test Plan	4/15/2011	✓		5/3/11
D005: Acceptance Test Report	5/3/2011	✓		5/6/11
D006: QA Audit Report	5/3/2011	✓		5/6/11
D007: Project Website	Periodically	✓		
D008: LPRDS-CMS-2011 Integrated System	5/6/2011	✓		5/6/11
D009: Conference Paper	4/8/2011	✓		5/3/11
D010: Project Poster	5/6/2011	✓		5/6/11

Introduction

In order to ensure the project can meet the requirements of the LPRDS-CMS-2011 Statement of Work, it must successfully pass acceptance testing. These tests will verify the various functions of the cell management system (CMS). The Acceptance Test Plan (ATP) gives step-by-step instructions on how to test the system to the fullest extent and make sure the CMS meets all the system requirements.

System Requirements

The project was originally presented with over 80 requirements. These were reviewed and several were not achievable/ applicable within the scope of the ECE 492 14-week term. The following are the agreed upon and altered requirements adapted from the LPRDS-CMS-2011 statement of work.

R002: Energy Storage

2. The existing ESS design does not allow any automated per-cell or aggregate battery management. There is no way to charge the cells individually taking into account their individual characteristics. *The LPRDS-CMS-2011 shall ~~re-engineer~~ design the ESS to permit per-cell battery management.*
3. The new system shall charge every cell ~~in the ESS~~ in the 4-cell pack to its maximum recommended capacity. Should some cells charge faster than others, a means shall be provided to bypass the cells that become full first, allowing complete charge to be delivered to cells that charge more slowly.
4. On discharge, every cell shall be monitored and over-discharge of any individual cell must be avoided.
5. The ESS shall be capable of standalone operation. It shall be possible to properly charge and discharge the ESS without needing an outside computer system for control or monitoring. Indicators shall be provided that give a basic display operational state (charge/discharge rate) and charge state (fuel gauge). Controls shall be provided, if needed, to permit standalone management.
8. In addition to local controls and indicators, a remote ~~SCADA~~ I^2C system shall be able to monitor in detail the voltage, and current of ~~, and state of charge of the aggregate ESS battery and~~ every individual cell in the CMS ~~ESS~~, as well as the overall state of charge of the pack ~~ESS parameters~~
9. Although a new charge-management system must be developed, the LPRDS-CMS-2011shall re-use the existing LiFePO4 cells incorporated in the existing ESS system. Also, to the largest extent possible, the existing mechanical enclosure, cabling, controls, and safety interfaces for the old ESS should be re-used.

GPR001: Documentation

1. Complete and accurate documentation must be provided with all projects. These documents shall include documents for mechanical and electrical fabrication, test results, software development kits, maintenance manual, user manual, and specification compliance matrices, and technical papers. All documentation shall be accumulated in electronic form, centralized in a project web site, and thoroughly indexed. The web site represents the primary point of delivery for document data items.
2. Text documents shall be written in a professional style commensurate with quality standards established by Lafayette College ECE writing courses (e.g. ES225 and ECE211).
3. All original paper documents should be scanned and stored electronically. The original should be disposed of per GPR012.
4. Test reports for hardware and software must show the date/time of testing, name and signature of the tester, and name/signature of any witnesses.

5. For all electronic PCB designs the following fabrication documents are required: dated, and numbered schematics or mechanical drawings on Lafayette College drawing format, circuit net-lists, bills of materials, artwork, assembly drawings, and all other files and instructions necessary for CAM or manual manufacturing. The source files for fabricating PCBs and editing linked schematics shall be clearly identified and preserved.
6. Documentation must be provided both for original designs and for any subcontracted designs. For purchased vendor components within the design, all vendor manuals and documentation shall be retained with the system. Proper mechanical drawings are required for fabricated mechanical parts. Manufacturers data sheets and interface drawings are required for all purchased components.
7. For software and firmware designs: Source code, and executable binaries for all applications; Verilog, constraints and configuration bitstreams for FPGAs; and ROM image files in commonly accepted JED or HEX formats for all PLDs.
8. A "Users" manual is required. This should be a high level document that explains all operational procedures and techniques needed to operate the system is a safe and effective manner, including "getting started", "FAQ", detailed explanations of all functions and controls, and user level calibration and maintenance.
9. A technical "Maintenance" manual is required. This should be a low level document that explains the unique technical principles and details of system operation. The maintenance manual includes information on any advanced maintenance or calibration techniques that could be applied by an expert maintainer. A set of schematics, pinouts of all connectors, the signal assignments of all cables, and the semantics of all interfaces (hardware and software) must be documented within this manual.
10. All documentation must be provided and delivered in electronic form. Emailing a description of a document along with a URL into the project web site is an acceptable and desirable form of delivery. The use of standard and portable document formats (*e.g.* PDF, TXT), must be used so that the documentation can be viewed on any computer without the need for proprietary applications. The documentation must be arranged in an organized and professional manner on the project web site.

GPR002: Environmental

1. All projects must demonstrate reliable and normal functional operation in ambient lab temperatures of 15 °C to 30 °C, 10% to 80% RH, non-condensing. The overall system must tolerate a storage environment of 0 °C to +60 °C, 5% to 95% RH, non-condensing. Designs should use electronic components rated for commercial temperature range (0 –70 °C) or better.

GPR003: EMI/EMC

1. Unintentional electromagnetic radiation radiated or conducted from designs must meet US CFR Title 47 Part 15 subpart B regulations for Class A digital equipment. Intentional radiators must meet subpart C regulations. Exemptions from 15.103 are not allowed.

GPR004: Hazmats

1. Hazardous materials should be avoided in designs. If use of a hazardous material is essential to the function of the design and there is no non-hazardous alternative, the use of the hazardous material must comply with the Lafayette College Chemical Hygiene Plan.
2. All materials used in electronic circuit fabrication must meet 2002/95/EC RoHS directives. NiCd or Lead-Acid batteries may not be used in new designs.

3. Any portion of the design or prototype that is discarded must be discarded according to the Lafayette College Chemical Hygiene plan. Also, projects should discard the collected electronic waste in an ecological-friendly manner as per the 2002/96/EC WEEE directive, either by ecological disposal or by reuse/refurbishment of the collected waste.

GPR005: Safety and Good Practice

1. All work shall comply with good industry practice that enhances reliability and maintainability. These practices include such items as
    - Color coded wiring in accordance with applicable industry standard color codes(*e.g.* NFPA 79 or UL508 for power wiring, EIA/TIA 568 for network wiring, etc...)
    - Clear labeling of all controls and indicators.
    - An obvious and clearly labeled system-wide power shutdown switch.
    - Silkscreen on PCBs that includes reference designators, noted power supply voltages and other critical signals. Silkscreen must show a Lafayette College logo, the words "Made in USA", a RoHS logo, assembly number and revision, and designated locations for serial numbers to be attached or written. PCB bottom copper should have text indicating the board part number and rev.
    - Fuses shall be socketed and at least 5 spares must be included with system delivery; breakers shall be resettable. All are readily accessible per maintainability requirements.
    - Service loops on all cable harnesses.
    - Access panels on enclosures.
2. Software/firmware developed must adhere to the principles and practice established in Lafayette College course CS205. Source code must be maintained under configuration control.
4. **Embedded computer processors shall have reset buttons. These buttons must be readily acceptable for maintenance, but not so easy to hit that they degrade reliability.**
5. Current drain analysis must be provided for all power supplies. Each supply voltage must have a current rating with a 50% safety factor over the anticipated peak current.
6. All resistors or other parts dissipating more than 25 milliwatts shall be identified and analysis shall be provided that shows all such parts are properly rated for peak and average power dissipation and have a proper heat sink and fan, if necessary, that provides adequate cooling over the ambient temperature range.
8. Components must be cooled such that the surface temperature is no greater than ~~40~~ 70 degrees C above ambient.
9. Power dissipation rating of parts shall be 50% overrated over the required temperature range.
10. Working voltage of capacitors shall be 25% overrated above the peak voltage anticipated, including all expected glitches, spikes, and tolerance limits.
11. Project activities must adhere to the general Lafayette College safety policy, possibly augmented by any ECE Department or ECE Laboratory safety rules. Applicable rules are those in effect on the date of ATP.

GPR006: Reliability

1. The system wide Mean Time Between Failures (MTBF) must be greater than 1000 hours over the system lifetime.
2. Reliability requirements must be demonstrated in the ATP both by analysis and by Inspection. The use of MIL-HDBK-217, Bellcore TR-332, or other equivalent techniques are encouraged for the analysis. Every part and subsystem in the full BOM must be explicitly considered in the MTBF analysis.
3. Parts with power dissipation over 25 milliwatts shall be identified and the reliability analysis shall include reliability derating of these components based on the expected dissipation.
4. **In addition to the analysis, a reliability inspection shall be conducted during ATP where the system is shown to operate for 24 hours without any obvious failure.**
5. Failures are defined as anything that causes system requirements to be missed. Failures include, but are not limited to computer software lock-ups, shutdowns caused by overheating, automatic operations stalled by exceptions or requests for human intervention, as well as random component failure.

GPR007: Maintainability

1. The system wide Mean Time To Repair (MTTR) must be less than 1 week over the system lifetime.
2. Maintainability requirements must be demonstrated in the ATP both by analysis and by Inspection. The use of MIL-HDBK-472 (N1) and MIL-STD-470B, ISO/IEC 25000:2005, or other equivalent techniques are encouraged for the analysis.
3. In the maintainability analysis you should assume a stock of recommended spare parts. The list of these spare parts should be included in the ATP. The Users Manual should include a section giving simple troubleshooting procedures. The Maintenance Manual should have more elaborate diagnosis and troubleshooting resources.
4. **In addition, a maintainability inspection shall be conducted during ATP where a novice using procedures included in the User Manual demonstrates the diagnosis and repair of a likely failure, and an expert using resources included in the Maintenance Manual demonstrates the diagnosis and repair of an UN-likely failure.**

GPR008: Manufacturability

1. A *production* design is a project design that could reasonably be manufactured in large quantity (*e.g.* greater than 1000 units/yr). All production designs must be built from components and subassemblies that have a sustainable source of supply over the system lifetime. To demonstrate that this requirement is met, it must be shown that each item in the Bill of Materials (BOM) for the design is available from a minimum of two independent suppliers. In addition, industry trends shall be considered when selecting 24 implementation options. Designs should choose options most aligned with future industry trends.
2. The tolerances of components shall be considered in the design. Any component with a value that determines a critical voltage, time constant, frequency, or other parameter shall have a tolerance such that system requirements are met with 99% yield in manufacturing. An analysis shall be provided that identifies any tolerance critical components and proves that the tolerances are adequate to meet system requirements at that yield.

GPR011: Project Demonstration

1. Completed projects must be demonstrated for review by ECE faculty.

GPR012: Final Disposal of Projects

1. Projects may be stored for future work, placed on display, or discarded. Time must be included in project schedules for final disposal.
2. If a project is to be stored, all its materials must be collected together in a single location. If possible, these materials should be enclosed in a sealed container, locked cabinet, or secure room that contains only these materials from one project and no other. If certain parts are impractical to store with the bulk of the project materials, these separate parts must be clearly labeled so their association with the stored project is obvious. Projects placed on display may have portions not on display. The undisplayed portions shall be either stored or discarded as described herein.
3. Portions of projects or complete projects that are discarded must be discarded in accordance with Hazmat procedures described herein.
4. Test equipment moved from labs shall be replaced in its original location.
5. Trash, loose wires, scattered components, and other detritus resulting from frenzied development and testing shall be cleaned up.
6. Paper documents that have been scanned per GPR001 shall be placed in a paper recycling bin.
7. The project web site must be updated with all final documents. The documents on the final web site must match the delivered system. Obsolete documents on the web site shall be removed.

In addition, the following special waivers and restrictions are applicable to the project:

Special Waivers and Restrictions (SWR001)

1. Analysis must show the system is compliant to GPR002; however, no formal environmental testing or empirical data is required.
2. Analysis can be used to show the system is compliant to GPR003; no formal EMI/EMC certification testing or empirical data is required.
3. Surface temperatures, supply current drains per GPR005 must be analytically predicted at CDR and physically measured and verified as compliant during ATP.
6. The system life for the purpose of requirements analysis other than for GPR009 shall be 5 years.

The first requirement of the LPRDS-CMS-2011 is to develop a new Energy Storage Subsystem (ESS) to replace the existing ESS. The main function of the ESS is to act as an Energy Accumulator to store the excess electrical energy available from the PC array and later deliver that stored energy to the Energy Delivery Subsystem (R002-1). The scope of this project is limited to a cell balancing PCB that is attached to each 4-cell pack. The system is scalable and can be used within the current ESS but will not be implemented or tested at this time. For this system, the SCADA interface is not used (R002-7). Instead an I^2C interface, which uses a USB adapter to communicate with a PC. Since we are reducing the scope of our project we cannot conform to ESS requirements inherited from previous years (R002-9, R002b-1 through R002b-13). Our project is not sophisticated enough for us to write a software application for interfacing with the pack (R006-1, R006-2). We also cannot write a demonstration

application on such a simple circuit (R008-1 through R008-5), however the OBPP board does demonstrate operation through the implementation of 4 LEDs demonstrating bypass and 3 LEDs indicating charging, discharging, and board status. We are not interfacing with any high voltage or photovoltaics (R009-1 through R009-3, R010-1, R010-2, SWR001-4, SWR001-5). In order to provide the ability to interface with the previous LPRDS system, the current system does include optical isolation for high voltage protection. We are not reusing previous year's safety interface (R011-1), but the redundant temperature safety system (RTSS) developed in this year's system is compatible with the safety loop developed by previous LPRDS projects. An electrical safety plan was written by previous LPRDS teams and adopted within the first week of the project (SWR001-7). We are not developing a DC potential difference greater than 30 Volts. A 4-cell battery pack produces around 12 Volts (GPR005-12). We are not designing our communication cables, power harnesses, or connectors according to NEC ANSI/NFPA 70 and ANSI C-2 (GPR005-13). We are not interfacing with the Lafayette college power grid (GPR005-14). We are not using lasers or any RF in our design (GPR005-15, GPR005-16). While the CMS will not operate by continually balancing a pack of cells for ECE department visitors, a demo program will be developed to show that the board design and integration on a pack of four cells produces a meaningful response from the firmware programmed onto the PIC microcontroller (GPR011-2).

Acceptance Test T001:

This test verifies the following requirements:

R002-2: The LPRDS-CMS-2011 shall ~~re-engineer the~~ design a new ESS to permit per-cell battery management

R002-3: The new system shall charge every cell ~~in the ESS~~ in the 4-cell pack to its maximum recommended capacity. Should some cells charge faster than others, a means shall be provided to bypass the cells that become full first, allowing complete charge to be delivered to cells that charge more slowly.

R002-4: On discharge, every cell shall be monitored and over-discharge of any individual cell must be avoided

R002-5: The ESS shall be capable of standalone operation. It shall be possible to properly charge and discharge the ESS without needing an outside computer system for control or monitoring. Indicators shall be provided that give a basic display operational state (charge/discharge rate) and charge state (fuel gauge). Controls shall be provided, if needed, to permit standalone management.

SWR001-3: Surface temperatures, supply current drains per GPR005 must be analytically predicted at CDR and physically measured (less than 70°C over ambient (30 °C)) and verified as compliant during ATP.

GPR005-8: Components must be cooled such that the surface temperature is no greater than 40degrees C above ambient.

Required Materials:

- MPJA 9604PS Power Supply
- Cell Management System (CMS)
  - 4-cell pack with OBPP (partially charged)
- (2) Gold SDP4040D DC Solid State Relay
- (4) 120 Watt 1-Ohm resistors
- IR Thermometer
- Alcohol Thermometer
- PC running Simulink
- National Instruments BNC2110 Data Acquisition Board
- Test Power Cables 1,2,3
- Test Data Cables 1,2,3
- Test Voltage Cables 1,2,3,4
- ~~Test Bypass Cables 1,2,3,4~~

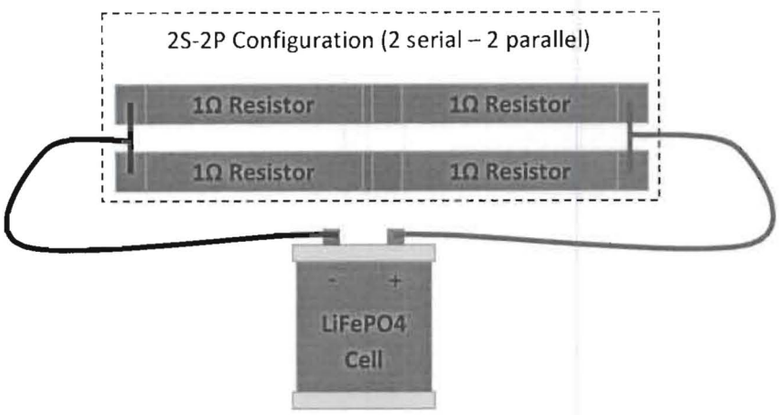


Figure 1

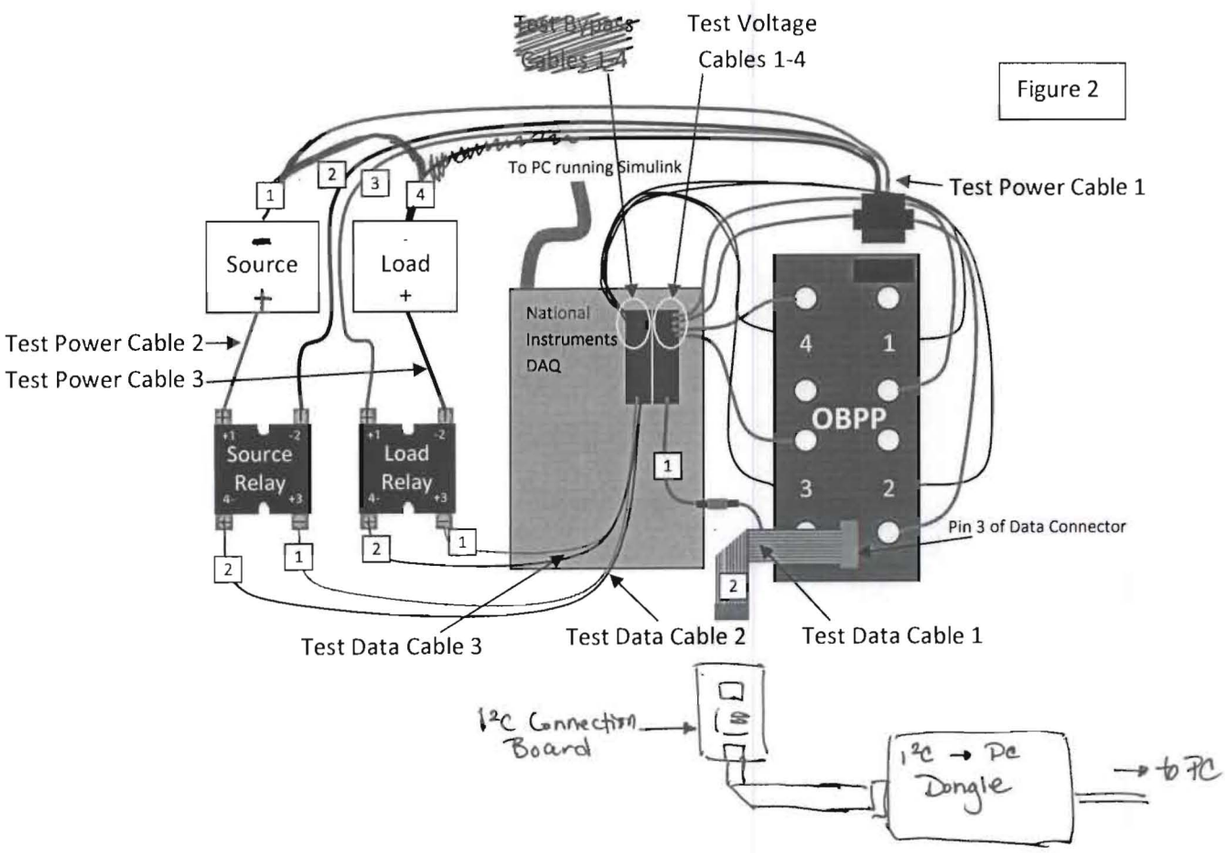


Figure 2

Test Procedure:

- Take 4 LiFePO4 cells and fully charge them individually using MPJA 9604PS Power Supply until each cell voltage reaches 3.8 V
- Discharge all the cells to the following SOCs: 80%, 50%, 25%, 10% by attaching ~~the~~ resistor ~~network in figure 1~~ to the two terminals of the battery cell for the specified amount of time: This distribution of SOCs represents a ~~27%~~ SOC standard deviation.

Cell	SOC (%)	Time (min)
1	~~80~~ 100	~~9~~ 0
2	~~50~~ 95	~~23~~ 20
3	~~25~~ 80	~~34~~ 40
4	~~10~~ 70	~~41~~ 60

- Connect the OBPP to the test system shown in figure 2
  - Connect wire 1 of Test Power Cable 1 to the ~~positive (+)~~ terminal of the source (MPJA 9604PS Power Supply)
  - Connect wire 2 of Test Power Cable 1 to the '-2' terminal of the 'Source Relay'
  - Connect wire 3 of Test Power Cable 1 to the '+1' terminal of the 'Load Relay'
  - Connect wire 4 of Test Power Cable 1 to the negative (-) terminal of the load (~~Transistor Devices RBL 400-600-4000 Variable Load~~)
  - Connect the ~~negative~~ terminal of the source to terminal '+1' of the 'Source Relay' using Test Power Cable 2.
  - Connect the positive terminal of the load to terminal '-2' of the 'Source Relay' using Test Power Cable 3.
  - Connect the common ground from the National Instruments DAQ board to terminal '4-' of the 'Source Relay' and 'Load Relay' using wires '2' of Test Data Cable 2 and Test Data Cable 3, respectively.
  - Connect wire '1' of Test Data Cable 2 from an output port of the DAQ to terminal '+3' of the 'Source Relay' and wire '1' of Test Data Cable 3 from an output port of the DAQ to terminal '+3' of the 'Load Relay'
  - Connect wire '1' of the data connector on the OBPP to an input port on the DAQ with a ~~22k~~ resistor ~~in series~~ using Test Data Cable 1. ~~Then connect the 5V ground on the DAQ to the same input port~~.
  - Connect the positive terminals of each of the cells to analog inputs 0-3 of the DAQ using Test Voltage Cables 1-4.
  - ~~Connect the positive leads of each of the bypass LEDs to analog inputs 1-4 of the DAQ using Test Bypass Cables 1-4.~~
- Using Simulink and the ~~previous~~ setup, the test will run for 5 charge/discharge cycles and record the voltage of the individual cells, demonstrating per-cell balancing within one pack.
  The Simulink file is named '~~top1.mdl~~' and is located on the project website under the tab "Resources" -> "Test Software".
- Set the MPJA 9604PS Power Supply to supply a 10A current to the CMS.
- Connect the 1Ω Resistors in a 2S-2P configuration as shown in figure 1 as the 'Load'

First Charge/Discharge Cycle

- The OBPP will initially charge the cells
- Observe that the yellow LED blinks to indicate that the OBPP is on

Yellow LED Flashes: (Pass) / Fail Initials: EA

- Set up scopes in Simulink to monitor the voltages from the four cells, the ~~bypass LEDs~~ and the 'done' signal. These ~~seven~~ five scopes will be used to analyze the operation of the pack.

R002-3 Following completion of the test, analysis of the data from the first charge/discharge cycle will be completed in ATR to demonstrate the operation of the bypass circuits.

Criteria for demonstrating operation of bypass is to show that if a cell is greater than 50mV from the lowest cell, the scope of the ~~LED for that~~ voltage cell will show a ~~jump~~ drop in voltage for a 20 min period. Full analysis for all cells for the full charge cycle will be completed in the ATR.

Second Charge/Discharge Cycle

- Observe when the cells are charging when a bypass LED is turned on, indicating partial resistive bypass. Using the IR heat gun & laser crosshairs, aim as close as possible towards the underside of the ~~board~~ heatSinks where the power resistors are located and find the maximum temperature.

SWR001-3
GPR005-8

Temp 1: 27 °C Temp 2: 24 °C Temp 3: 25 °C Temp 4: 27 °C

Within 70°C above 30°C ambient: (Pass) / Fail Initials: EA

- Wait 15 minutes and repeat previous step again.

SWR001-3
GPR005-8

Temp 1: 33.5 °C Temp 2: 35.2 °C Temp 3: 30 °C Temp 4: 31 °C

Within 70°C above 30°C ambient: (Pass) / Fail Initials: EA

- Wait 15 minutes and repeat step a third time.

SWR001-3
GPR005-8

Temp 1: 34.7 °C Temp 2: 36.9 °C Temp 3: 33.5 °C Temp 4: 32.6 °C

Within 70°C above 30°C ambient: (Pass) / Fail Initials: EA

- ~~Once the second charge/discharge cycle has completed, stop the Simulink file and save the information collected. Restart the file once the previous data has been saved.~~
  ~~* Following every two (2) charge/discharge cycles, stop the Simulink file and save a backup of the information collected during that time.~~

Fifth

Third-~~Tenth~~ Charge/Discharge Cycles

- Monitor temperature of board once at end of every charging cycle to make sure that board does not exceed temperature requirements:

SWR001-3
GPR005-8

Cycle 3: 50 °C Cycle 4: 43 °C Cycle 5: 42 °C

Within 70°C above 30°C ambient: (Pass) / Fail Initials: EA

- Following the completion of the all five (5) charge/discharge cycles, look at the voltage curve data which the Simulink test collected.

- Identify that the standard deviation of the states of charge over the period of 5 charge/discharge cycles decreased by the following analysis:

  Once the cells have finished the 5 charge/discharge cycles, remove cells from pack and individually charge them to capacity (Vmax being set at 3.8V) by attaching each individual cell to the MPJA 9604PS Power Supply and setting the current to 10A. Record the time required to charge each cell to its maximum voltage:

  Cell 1: 0.1844 hrs Cell 2: 0.2261 hrs Cell 3: 0.2625 hrs Cell 4: 0.0128 hrs

- Multiply the time to top-off by the current used to charge the cells to get the amount of SOC still uncharged in each of the cells. Subtract each of these numbers from the capacity of the cell (10 A-hr) and divide by the cell capacity and multiply by 100 to get the SOC of each cell at the eand of the five (5) charge/discharge cycles:

  Uncharged Capacity:

  Cell 1: 1.844 A-hr Cell 2: 2.261 A-hr Cell 3: 2.625 A-hr Cell 4: 0.128 A-hr

  Ending State of Charge:

$$\frac{10\ Amp \cdot hrs - x}{10\ Amp \cdot hrs} \times 100 = SOC$$

  Cell 1: $x_1 =$ 81.56 % Cell 2: $x_2 =$ 77.39 % Cell 3: $x_3 =$ 73.75 % Cell 4: $x_4 =$ 98.72 %

  Compute the average SOCs of the four cells: $\bar{x} =$ 82.86 %

- Compute the standard deviation of the cells in the pack by the following formula:

$$\sigma = \sqrt{\frac{(x_1-\bar{x})^2+(x_2-\bar{x})^2+(x_3-\bar{x})^2+(x_4-\bar{x})^2}{4}} =$$ 9.57 % SOC

  Is the final standard deviation of the cells within the pack less than the standard deviation at the beginning of the test (27%)?

R002-2 (Pass) / Fail Initials: EA

- After the last charge/discharge cycle, allow the pack to sit without balancing overnight. If there is more time left in the 24-hour period of the test, continue to observe the board and look for failure conditions.

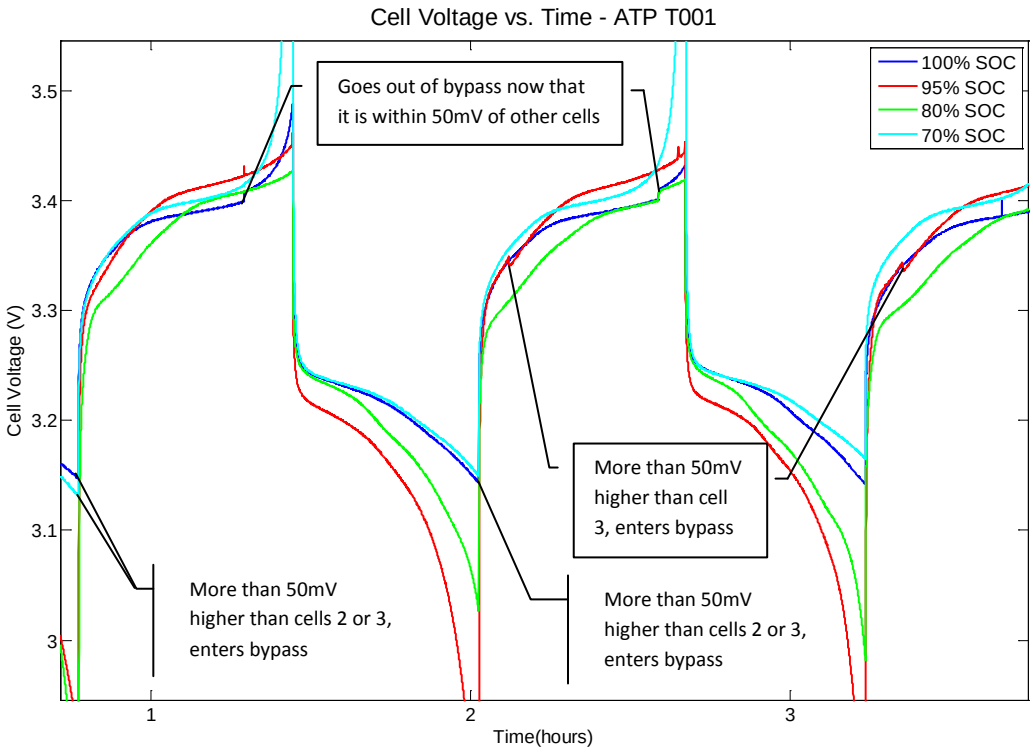
GPR006-4	Does system runs without failure*:	Pass / Fail	Initials: EA

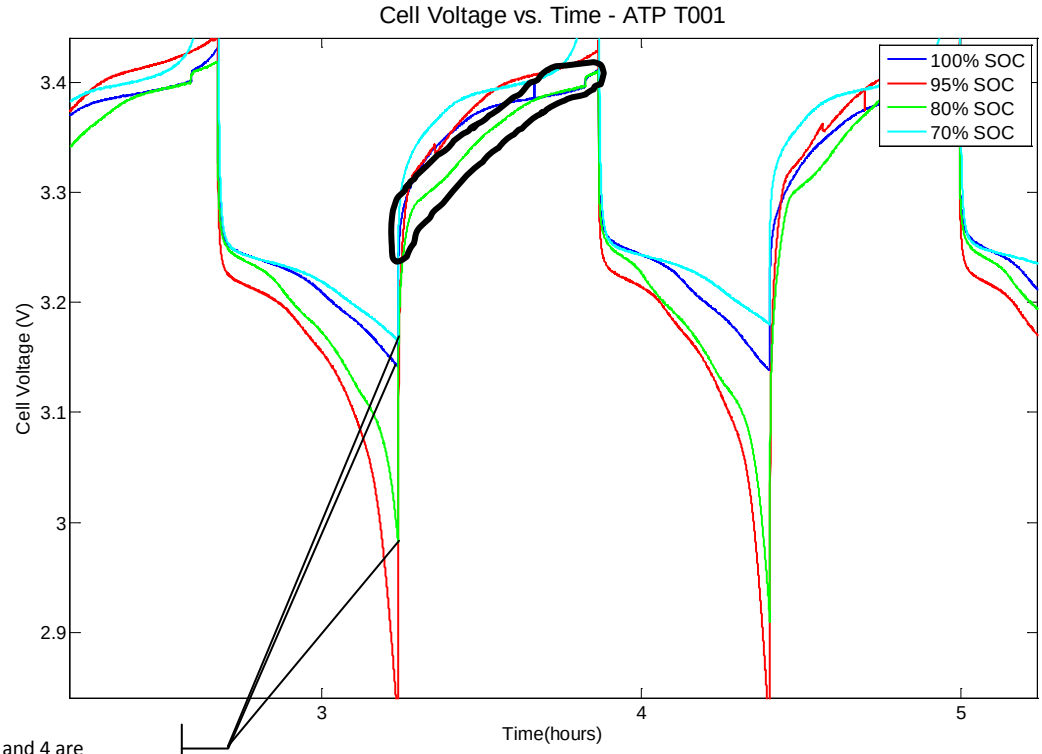
*Failure is defined as the following conditions for board and software:

Board failure: overheating beyond specified threshold temperature, discoloration, combustion or other obvious component failure.

Software failure: relays cease to function and charging/discharging indicators fail to update over the expected duration of a cycle. Further software failure can occur in I2C communication, which will be tested in T002.

ATP T001 – Verification of Operation of Bypass





Cells 1, 3 and 4 are 300mV, 325mV and 125mVhigher than cell 2, Enters bypass

Acceptance Test T002:

This test verifies the following requirements:

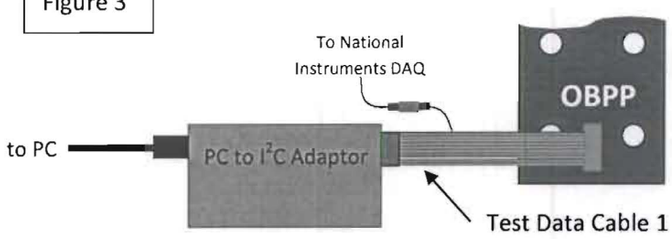
R002-6: In addition to local controls and indicators, a remote ~~SCADA~~ I^2C system shall be able to monitor in detail the voltage, and current of ~~, and state of charge of the aggregate ESS battery and~~ every individual cell in the CMS ~~ESS~~, as well as the overall state of charge of the pack ~~ESS parameters~~

R002-5: The ESS shall be capable of standalone operation. It shall be possible to properly charge and discharge the ESS without needing an outside computer system for control or monitoring. Indicators shall be provided that give a basic display operational state (charge/discharge rate) and charge state (fuel gauge). Controls shall be provided, if needed, to permit standalone management.

Required Materials:

- MPJA 9604PS Power Supply
- Cell Management System (CMS)
  - 4-cell pack with OBPP (partially charged)
- (2) Gold SDP4040D DC Solid State Relay
- (4) 120 Watt 1-Ohm resistors
- PC running Simulink & RealTerm
- National Instruments BNC2110 Data Acquisition Board
- Test Power Cables 1,2,3
- Test Data Cables 1,2,3
- Test Voltage Cables 1,2,3,4
- Test Bypass Cables 1,2,3,4
- PC to I2C Adaptor (utilizing USB)
- Agilent Digital Multimeter 34401A
- 16710 TE Infrared Thermometer

Figure 3



Test Procedure:

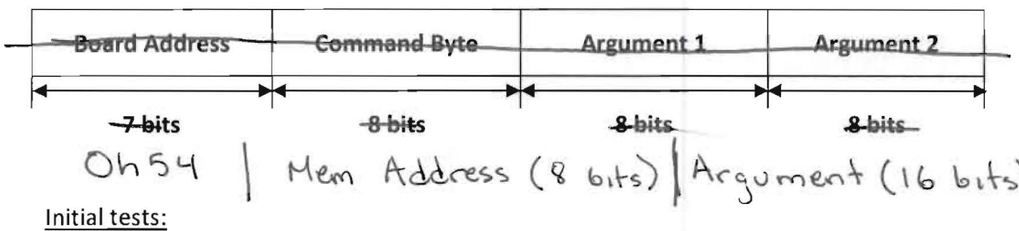
- Maintain the same connection configuration as shown in figure 2 with the following exception:
  - Connect the red connector of 'Test Data Cable 1' to the 'PC to I2C' Adaptor as displayed in Figure 3 to enable I2C communication

- Begin the program RealTerm on the PC, click on the tab which says I2C in order to test the functionality of the communication.

- The OBPP will begin charging the pack of cells as an initialization cycle

- I2C commands are formed by three bytes of information:

I2C Command Format



0h54 | Mem Address (8 bits) | Argument (16 bits)

Initial tests:

- Change the I2C address of the board currently connected to the I2C interface to be board ~~0x08~~ 0h0008 with the following command in RealTerm:
  - Write I2C Address: ~~00000000 00000000 00010000~~ 0h54100008

- Query the I2C for the Board Number and Firmware Version ID with the following command in RealTerm to confirm that the change of I2C address was successful
  - Read Board Number: ~~00010000 00000001 00011001~~ 0h081BF000
  - Read Version ID: ~~00010000 00000001 00011000~~ 0h081AF000

R002-6

Version ID: ~~0x10~~ 0h0010 (Pass) / Fail Initials: EA

Board Number: ~~0x15~~ 0h0001 (Pass) / Fail Initials: EA

Voltage Tests

- Query via I2C for the voltages of the 4 cells by typing in the following commands into RealTerm:
  - Read Voltage 1: ~~00010000 00000001 00000001~~ 0h0801F000
  - Read Voltage 2: ~~00010000 00000001 00000010~~ 0h0802F000
  - Read Voltage 3: ~~00010000 00000001 00000011~~ 0h0803F000
  - Read Voltage 4: ~~00010000 00000001 00000100~~ 0h0804F000

I2C V1: 3.34 V (AB2) I2C V2: 3.36 V (AC1) I2C V3: 3.38 V (ACF) I2C V4: 3.36 V (ABF)

- Manually measure the voltages across the terminals of each cell in the CMS
  DMM V1: 3.33 V DMM V2: 3.34 V DMM V3: 3.34 V DMM V4: 3.34 V

SOC & Current Tests

- Query I2C for the integrated current of the pack and time step by entering the following commands into RealTerm.
  - Because the system was originally designed for the master device to do the calculations for aggregate battery pack SOC, the number which is returned by this query is not the actual SOC of the pack. The number returned is the average current which passed through the cell for the duration of the charge/discharge cycle.
  - Read I_{INT}: ~~00010000 00000001 00001001~~ 0h0809F000
  - ~~Read T:~~ ~~00010000 00000001 00011010~~ [redacted]

I_{INT}: [redacted] 340A T: 31 min

$$\frac{I_{INT} \times T}{capacity} \times 100 = \frac{340\ A \times 31\ /60\ hr}{10\ A \cdot h} \times 100 = 56.6\%$$

Observe the current indicator on the MPJA 9604PS Power Supply. Record the value, this will be used as average current to calculate SOC. Record the amount of time that this charge cycle took to complete, enter values into the following formula and calculate:

$$\frac{I_{AVG} \times Time}{capacity} \times 100 = \frac{\_\_\_\ A \times \_\_\_\ hr}{10\ A \cdot h} \times 100 = \_\_\_\%$$

SOC from I2C and observation differ by less than 10% Pass / (Fail) Initials: JB

- Query I2C for the current of the pack by entering the following command into RealTerm:
  - Read current: ~~00010000 00000001 00000000~~ 0h0800F000

I2C Current: 4.75 (0985) A

- Observe the current indicator on the MPJA 9604PS Power Supply. Test whether the I2C current is within 10% C (~~1~~ 500mA) of the Power Supply current.

PS Current: 5 A I2C ± 1A = PS (Pass) / Fail Initials: [redacted]

Temperature Test 1

- Query I2C for the temperatures of the 4 cells by entering the following commands into RealTerm:
  - Read Temp 1: ~~00010000 00000001 00000101~~ 0h0805F000
  - Read Temp 2: ~~00010000 00000001 00000110~~ 0h0806F000
  - Read Temp 3: ~~00010000 00000001 00000111~~ 0h0807F000
  - Read Temp 4: ~~00010000 00000001 00001000~~ 0h0808F000

I2C T1: 26.7 (70A) °C I2C T2: 22.3 (6A0) °C I2C T3: 24.2 (6D2) °C I2C T4: 25.2 (6E4) °C

- Manually measure the temperatures of areas near each of the temp sensors on the OBPP using the 16710 TE Infrared Thermometer

IR T1: 23.9 °C IR T2: 22.2 °C IR T3: 22.2 °C IR T4: 22.8 °C

PUT IN MANUAL MODE:

0h0812000FF

Master Device Test 1

- Query I2C and set all power resistors in bypass for 5 minutes with the following commands in RealTerm:
  - Bypass Switch 1: ~~00010000 00000000 00001010 00001011~~ 0h080B000B
  - Bypass Switch 2: ~~00010000 00000000 00001011 00001011~~ 0h080C000B
  - Bypass Switch 3: ~~00010000 00000000 00001100 00001011~~ 0h080D000B
  - Bypass Switch 4: ~~00010000 00000000 00001101 00001011~~ 0h080E000B

R002-6 Red Bypass LEDs turned on for 5 min ± 30 sec: (Pass) / Fail Initials: EA

- Setting the ~~resistors in bypass causes the~~ board to go into "non-automatic" mode. Observe that the yellow "status" LED no longer pulses, but remains solid, indicating "non-automatic" mode.

R002-6 Yellow LED solid: (Pass) / Fail Initials: EA

Temperature Test 2

- Query I2C for the temperatures of the 4 cells and manually measure temperatures of areas near each of the temp sensors on the OBPP as in Temperature Test 1:

I2C T1: 31.4 (~~77B~~) °C I2C T2: 33.7 (7B4) °C I2C T3: 35.3 (7DA) °C I2C T4: 35.7 (7E5) °C

IR T1: 27.4 °C IR T2: 24.5 °C IR T3: 24.0 °C IR T4: 25.9 °C

Subtract temperatures from Temperatures Test 1 from Temperature Test 2 for both I2C and IR:

I2C:
Diff 1: 4.7 °C Diff 2: 11.4 °C Diff 3: 11.1 °C Diff 4: 10.2 °C

IR:
Diff 1: 3.5 °C Diff 2: 2.3 °C Diff 3: 1.8 °C Diff 4: 3.1 °C

Differences between I2C & IR are no greater than 10% of highest of the two values

Diff 1: Pass / (Fail) Diff 1: Pass / (Fail) Diff 3: Pass / (Fail) Diff 1: Pass / (Fail)

Initials: EA

Master Device Test 2

- Query I2C and set board back to 'automatic mode' with the following command with RealTerm
  - Enter Automatic Mode: ~~00010000 00000100~~ 0h0812000O

- Query I2C and determine which mode the system is in (automatic/not) with the following command in RealTerm:
  - Get Mode: ~~00010000 00000001 00010001~~ 0h0812F000

R002-6 Does RealTerm return ~~0xFF~~ 0h0000? (Pass) / Fail Initials: EA

Yellow LED ~~solid~~ blinking (Pass) / Fail Initials: EA

Does system runs without failure*: (Pass) / Fail Initials: EA

*Board failure criteria are the same as in T001

*Software failure: I2C commands remain responsive throughout test.

Novice: Greg Brasiello: Greg Brasiello

Acceptance Test T003:

- Cause a common failure in the system and allow a novice to utilize the **User Manual** in troubleshooting and solving the problem.
    - A CMS is set up so that the fuse located on the board is one which has been burned out in a previous experiment being conducted for QA testing. The novice is not aware of this fact.
    - Tell the novice that when the board is correctly hooked up that there is no output from the power connector, but that the microprocessor is still operating, and can still communicate via I2C.
    - The novice is given the User Manual for the LPRDS-CMS-2011 system and asked to troubleshoot the malfunctioning board by reading the User Manual and determining that the reason the board is not working is because of the burned out fuse.

R006-4	Novice was able to solve problem: (Pass) / Fail	Initials: GE

- Cause an uncommon failure in the system and allow a system expert to utilize the **Maintenance Manual** in troubleshooting and solving the problem.

R006-4	Expert was able to solve problem: (Pass) / Fail	Initials: GE

Expert: Eric Adolfsson: Eric Adolfsson

ATP Test T003:

Expert: Erik Adolfsson
Witness: Will Schlansker
Date: 5/5/11

The pack was first connected to the relays and put into the discharge state. The red discharging LED blinked a few times and then went solid to indicate the pack was empty. The resistive load was removed from the pack and I used a multi-meter to measure the voltage of the pack and concluded that it was in fact, not empty. Next, the expert measured the voltage of each cell and compared each of these values to the corresponding I2C value. It was immediately apparent that the I2C value for cell 1 did not match the multi-meter. The expert used the Maintenance Manual to find the appropriate pin for cell 1 voltage and I checked the input pin to the A2D for cell 1 and saw that it matched the I2C but not the multi-meter. The expert then narrowed his focus to the differential amplifier between the voltage for cell 1 and the PIC. He removed the OBPP from the battery pack and pulled up the schematic for the differential amplifier. He located the differential amplifier for cell 1 and I inspected the chip. It looked burnt out but to be sure he inspected the resistor values. All 4 resistors in the circuit are 100K. The expert used the multi-meter to confirm this and then deduced the TLC-2252 chip was faulty and needed replacement. Once the chip was replaced, the cell 1 voltage input to the A2D was restored to the proper value.